

North South University

Center of Excellence in Higher Education

CSE231.2

Term Project-SP18

Phase 2: Sequential Circuit design

Group : **7**

Group Members:

|  |  |
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Submitted to:

**Dr. Arshad M. Chowdhury**

Submission date: 23.03.2018

**Objectives:**

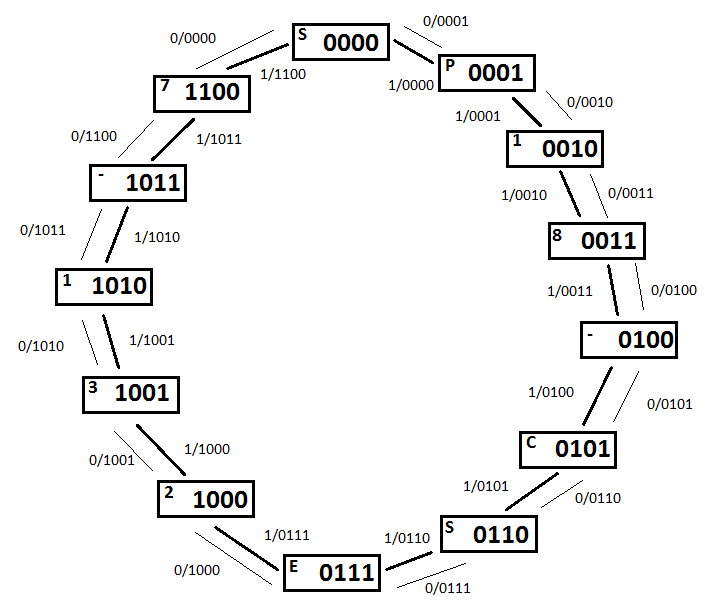
* To design the sequential logic part of the system
* Design a complete logic system from specification to implementation
* Coordination between the combinational and the sequential parts
* Become familiarized with the analysis of combinational logic networks and Synchronous Sequential Logic
* Learn the implementation of networks using Logic gates, decoders or MUX
* We need to display “**SP18-CSE231-7**” if the Direction input is logic **LOW** and the reverse order (“**7-132ESC-81PS**”) if the Direction input is logic **HIGH**

**Phase 2: Sequential Circuit design**

**List of Equipment:**

* IC 7473 (JK Flip-Flop) - 2 piece
* IC 7421 (4-input AND gate) - 1 piece
* IC 7411 (3-input AND gate) - 2 piece
* IC 7408 (2-input AND gate) - 2 piece
* IC 4072 (4-input OR gate) - 1 piece
* IC 4075 (3-input OR gate) - 1 piece
* IC 7432 (2-input OR gate) - 1 piece
* IC 7404 (NOT Gates) - 1 piece
* Voltage Regulator
* Voltage source
* Breadboard
* Switch
* Wires

**State Diagram:**

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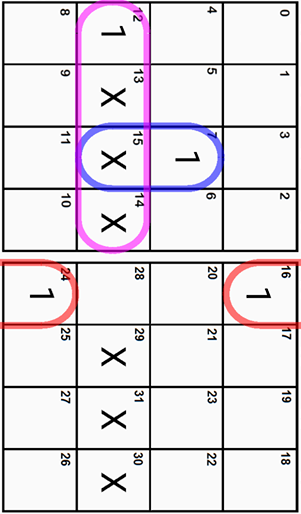
**State Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | **Present State** | | | | |  | **Next State** | | | | |  | **Flip Flop Inputs** | | | |
| **A** | **State** | **Bt** | **Ct** | **Dt** | **Et** | **State** | **Bt+1** | **Ct+1** | **Dt+1** | **Et+1** | **TB** | **TC** | **TD** | **TE** |
| 0 | S | 0 | 0 | 0 | 0 |  | P | 0 | 0 | 0 | 1 |  | 0 | 0 | 0 | 1 |
| 0 | P | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 8 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 8 | 0 | 0 | 1 | 1 | - | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | - | 0 | 1 | 0 | 0 | C | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | C | 0 | 1 | 0 | 1 | S | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | S | 0 | 1 | 1 | 0 | E | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | E | 0 | 1 | 1 | 1 | 2 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 2 | 1 | 0 | 0 | 0 | 3 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 3 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | - | 1 | 0 | 1 | 1 | 7 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 7 | 1 | 1 | 0 | 0 | S | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 |  | 1 | 1 | 0 | 1 |  | X | X | X | X | X | X | X | X |
| 0 |  | 1 | 1 | 1 | 0 |  | X | X | X | X | X | X | X | X |
| 0 |  | 1 | 1 | 1 | 1 |  | X | X | X | X | X | X | X | X |

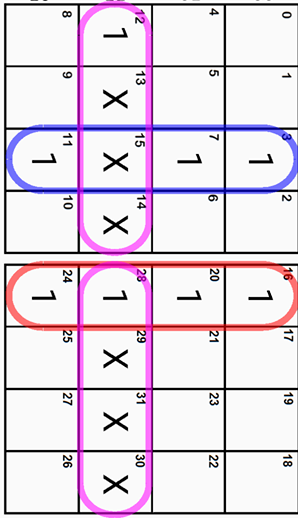
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | **Present State** | | | | |  | **Next State** | | | | |  | **Flip Flop Inputs** | | | |
| **A** | **State** | **Bt** | **Ct** | **Dt** | **Et** | **State** | **Bt+1** | **Ct+1** | **Dt+1** | **Et+1** | **TB** | **TC** | **TD** | **TE** |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | S | 0 | 0 | 0 | 0 |  | 7 | 1 | 1 | 0 | 0 |  | 1 | 1 | 0 | 0 |
| 1 | P | 0 | 0 | 0 | 1 | S | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | P | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 8 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | - | 0 | 1 | 0 | 0 | 8 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | C | 0 | 1 | 0 | 1 | - | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | S | 0 | 1 | 1 | 0 | C | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | E | 0 | 1 | 1 | 1 | S | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 2 | 1 | 0 | 0 | 0 | E | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 3 | 1 | 0 | 0 | 1 | 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 3 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | - | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 7 | 1 | 1 | 0 | 0 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 |  | 1 | 1 | 0 | 1 |  | X | X | X | X | X | X | X | X |
| 1 |  | 1 | 1 | 1 | 0 |  | X | X | X | X | X | X | X | X |
| 1 |  | 1 | 1 | 1 | 1 |  | X | X | X | X | X | X | X | X |

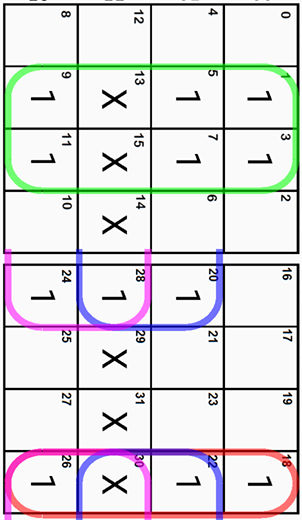
**Karnaugh map (K-map):**

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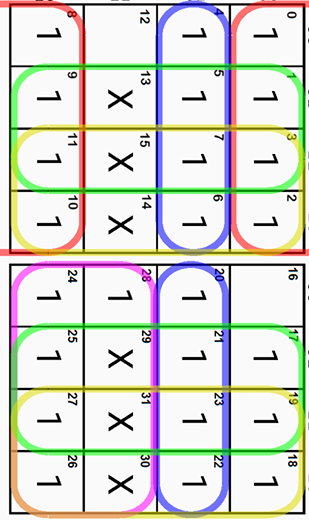
**TB = **

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**TC = **

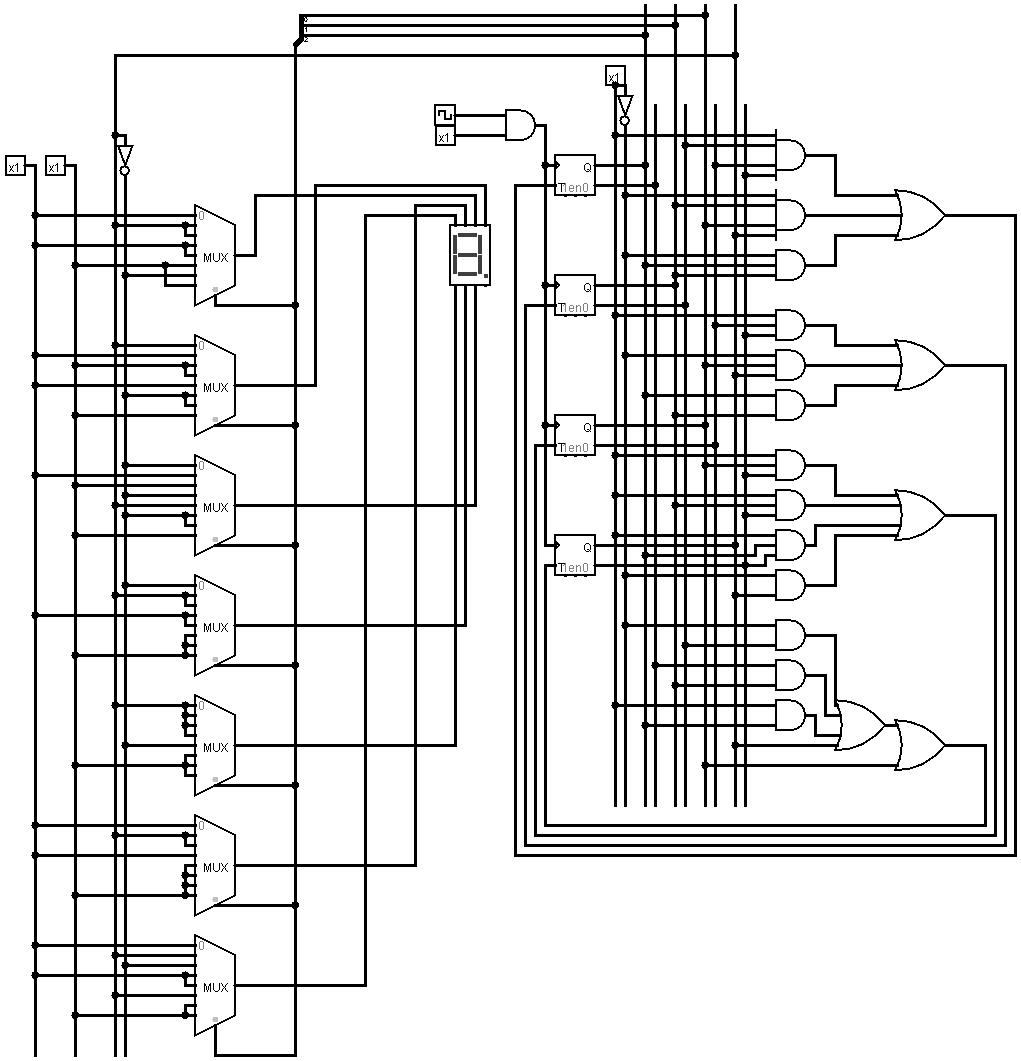
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**TD = **

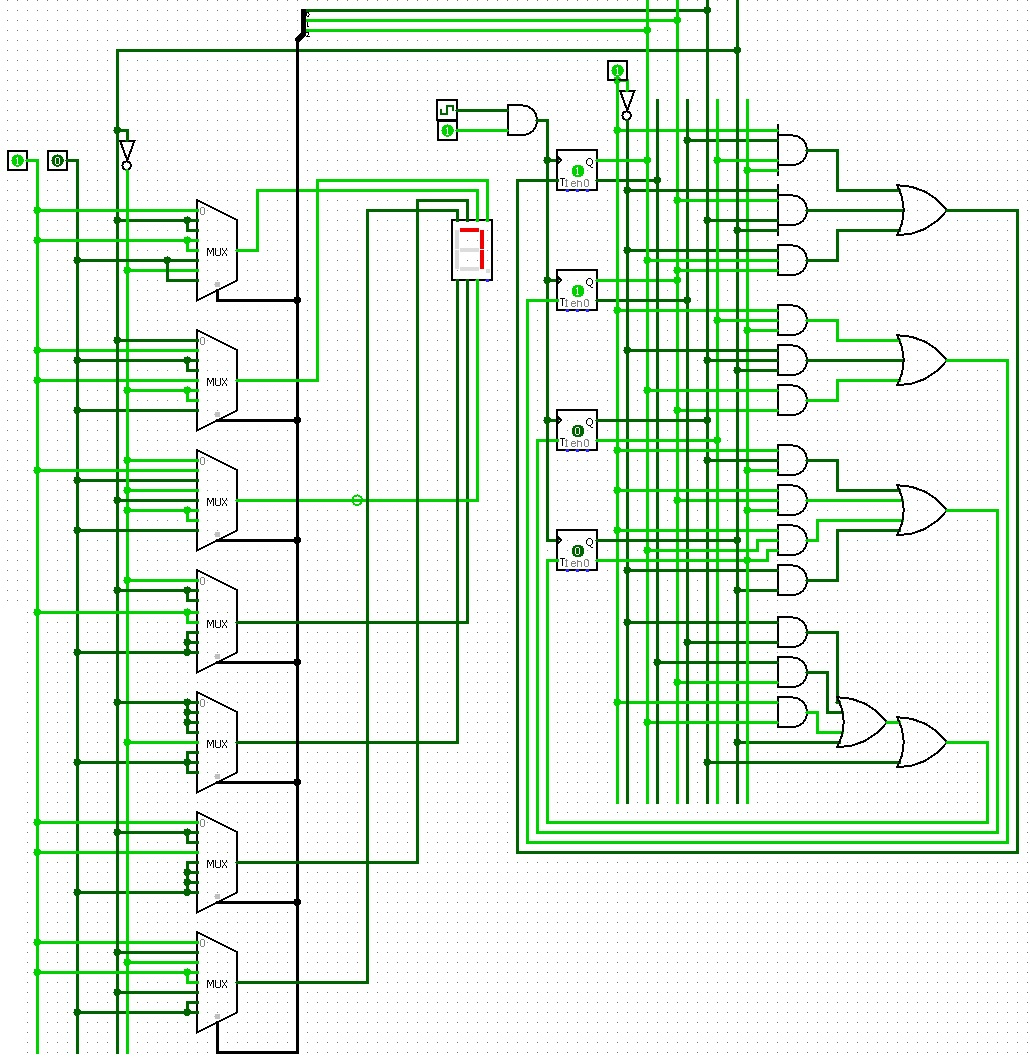
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**TE = **

**Circuit Diagram :**

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**Simulation :**

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**Explanation**:

Upon analysis of the table, it was clear that **T** Flip Flops would give a simplified circuit. However, T FFs were not available in the market so we decided to make **T** Flip Flops using **JK** Flip Flop. Behind this decision we had to consider a few facts for instance

efficiency, complexity, cost consideration etc.

From the figure we found that for both **D** Flip Flop and **JK** the Literal cost (L), Gate input cost (G), Gate input cost including inverters (GN) are much higher than the **T** Flip Flops. Also it will be a very complicated circuit where relatively more wiring is required and also the cost of implementation is higher. Thus we have decided to use **T** Flip Flops to implement the circuit.